Atmel SAM C21E / SAM C21G / SAM C21J

SMART ARM-Based Microcontroller

PRELIMINARY DATASHEET SUMMARY

Description

The Atmel® | SMART™ SAM C21 is a microcontroller series optimized for industrial automation, appliances and other 5V applications using the 32-bit ARM® Cortex®-M0+ processor, and ranging from 32- to 64-pins with up to 256KB Flash and 32KB of SRAM. The SAM C21 devices operate at a maximum frequency of 48MHz and reach 2.46 Coremark/MHz. They are designed for simple and intuitive migration with identical peripheral modules, hex compatible code, identical linear address map and pin compatible migration paths between all devices in the product series. All devices include intelligent and flexible peripherals, Atmel Event System for inter-peripheral signaling, and support for capacitive touch button, slider and wheel user interfaces. SAM C21 devices are pin compatible to the SAM D family of general purpose microcontrollers.

The Atmel SAM C21 devices provide the following features: In-system programmable Flash, twelve-channel direct memory access (DMA) controller, twelve channel Event System, programmable interrupt controller, up to 52 programmable I/O pins, 32-bit real-time clock and calendar, up to five 16-bit Timer/Counters (TC) and three Timer/Counters for Control (TCC), where each TC can be configured to perform frequency and waveform generation, accurate program execution timing or input capture with time and frequency measurement of digital signals. The TCs can operate in 8- or 16-bit mode, selected TCs can be cascaded to form a 32-bit TC, and three timer/counters have extended functions optimized for motor, lighting and other control applications. Two TCC can operate in 24-bit mode, and the third TCC can operate in 16-bit mode. The series provide two Controller Area Network (CAN) modules supported CAN 2.0A/B and CAN-FD 1.0; up to six Serial Communication Modules (SERCOM) that each can be configured to act as an USART, UART, SPI, I^2C up to 3.4MHz, SMBus, PMBus, RS-485 and LIN master/slave; two 12-bit, 1Msps ADCs with up to 12-channels each (20 unique channels total), one 10-bit 300ksps DAC, four analog comparators with window mode, Peripheral Touch Controller supporting up to 256 buttons, sliders, wheels and proximity sensing; programmable Watchdog Timer, brown-out detector and power-on reset and two-pin Serial Wire Debug (SWD) program and debug interface.

All devices have accurate and low-power external and internal oscillators. All oscillators can be used as a source for the system clock. Different clock domains can be independently configured to run at different frequencies, enabling power saving by running each peripheral at its optimal clock frequency, and thus maintaining a high CPU frequency while reducing power consumption.

The SAM C21 devices have three software-selectable sleep modes, idle, standby and off. In idle mode the CPU is stopped while all other functions can be kept running. In standby all clocks and functions are stopped expect those selected to continue running. In this mode all RAMs and logic contents are retained. The device supports SleepWalking. This feature allows the peripheral to wake up from sleep based on predefined conditions, and thus allows some internal operation like DMA transfer and/or the CPU to wake up only when needed, e.g. when a threshold is crossed or a result is ready. The Event System supports synchronous and asynchronous events, allowing peripherals to receive, react to and send events even in standby mode.

The Flash program memory can be reprogrammed in-system through the SWD interface. The same interface can be used for non-intrusive on-chip debug of application code. A boot loader running in the device can use any communication interface to download and upgrade the application program in the Flash memory.

The Atmel SAM C21 devices are supported with a full suite of program and system development tools, including C compilers, macro assemblers, program debugger/simulators, programmers and evaluation kits.

Features

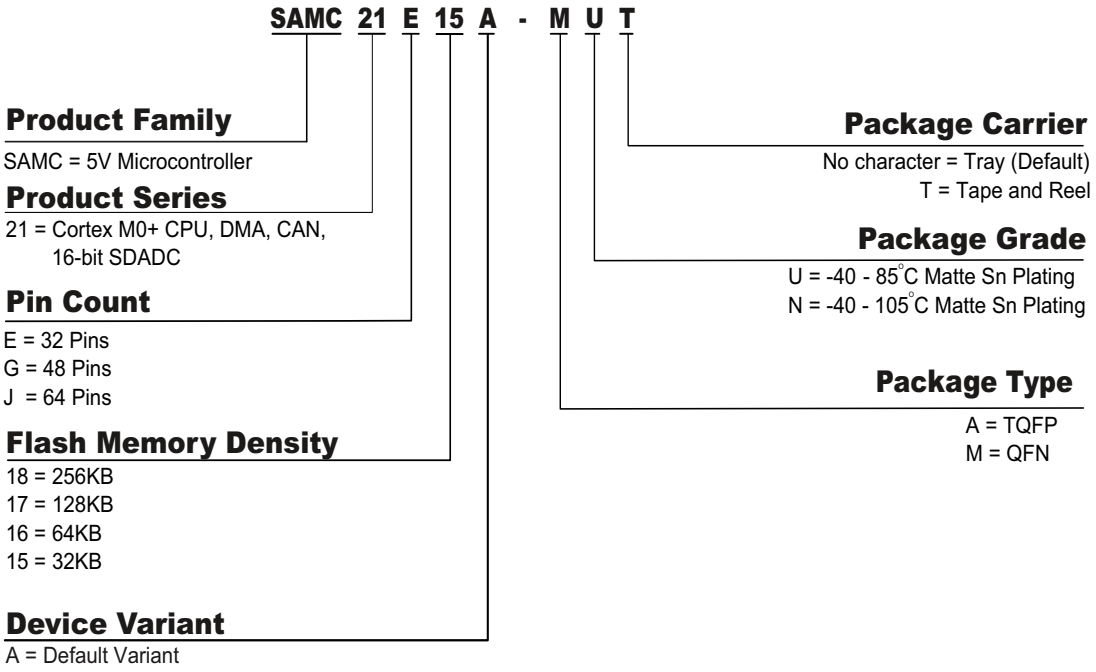
- Processor
  - ARM Cortex-M0+ CPU running at up to 48MHz
    - Single-cycle hardware multiplier
    - Micro Trace Buffer
- Memories
  - 32/64/128/256KB in-system self-programmable Flash
  - 2/4/6/8KB independent self-programmable Flash for EEPROM emulation
  - 4/8/16/32KB SRAM Main Memory
- System
  - Power-on reset (POR) and brown-out detection (BOD)
  - Internal and external clock options with 48MHz to 96MHz Fractional Digital Phase Locked Loop (FDPLL96M)
  - External Interrupt Controller (EIC)
  - 16 external interrupts
  - One non-maskable interrupt
  - Two-pin Serial Wire Debug (SWD) programming, test and debugging interface
- Low Power
  - Idle, standby, and off sleep modes
  - SleepWalking peripherals
- Peripherals
  - Hardware Divide and Square Root Accelerator (DIVAS)
  - 12-channel Direct Memory Access Controller (DMAC)
  - 12-channel Event System
  - Up to five 16-bit Timer/Counters (TC), configurable as either:
    - One 16-bit TC with compare/capture channels
    - One 8-bit TC with compare/capture channels
    - One 32-bit TC with compare/capture channels, by using two TCs
  - Two 24-bit and one 16-bit Timer/Counters for Control (TCC), with extended functions:
    - Up to four compare channels with optional complementary output
    - Generation of synchronized pulse width modulation (PWM) pattern across port pins
    - Deterministic fault protection, fast decay and configurable dead-time between complementary output
    - Dithering that increase resolution with up to 5 bit and reduce quantization error
  - 32-bit Real Time Counter (RTC) with clock/calendar function
  - Watchdog Timer (WDT)
  - CRC-32 generator
  - Up to two Controller Area Network (CAN) interfaces
    - CAN 2.0A/B
    - CAN-FD 1.0
  - Up to six Serial Communication Interfaces (SERCOM), each configurable to operate as either:
    - USART with full-duplex and single-wire half-duplex configuration
    - I^2C up to 3.4MHz
    - SPI
    - LIN master/slave
    - RS-485
  - One Configurable Custom Logic (CCL)
  - Two 12-bit, 1Msps Analog-to-Digital Converter (ADC) with up to 12-channels each (20 unique channels total)
    - Differential and single-ended input
    - Automatic offset and gain error compensation
    - Oversampling and decimation in hardware to support 13-, 14-, 15- or 16-bit resolution
  - One 16-bit, 1ksps Sigma-Delta Analog-to-Digital Converter (SDADC) with up to 3 differential channels
  - 10-bit, 300ksps Digital-to-Analog Converter (DAC)
    - Hardware support for 14-bit using dithering
  - Four Analog Comparators (AC) with window compare function
  - Integrated Temperature Sensor with ±1°C accuracy
  - Peripheral Touch Controller (PTC)
    - 256-Channel capacitive touch and proximity sensing
- I/O
  - Up to 52 programmable I/O pins
- Drop in compatible with SAM D20 and SAM D21
- Packages
  - 64-pin TQFP, QFN
  - 48-pin TQFP, QFN
  - 32-pin TQFP, QFN
- Operating Voltage
  - 2.7V – 5.5V

1. Configuration Summary

	SAM C21J	SAM C21G	SAM C21E
Pins	64	48	32
General Purpose I/O-pins (GPIOs)	52	38	26
Flash	256/128/64/32KB	256/128/64/32KB	256/128/64/32KB
Flash RWW section	8/4/2/1KB	8/4/2/1KB	8/4/2/1KB
System SRAM	32/16/8/4KB	32/16/8/4KB	32/16/8/4KB
Timer Counter (TC) instances	5	5	5
Waveform output channels per TC instance	2	2	2
Timer Counter for Control (TCC) instances	3	3	3
Waveform output channels per TCC	8/4/2	8/4/2	6/4/2
DMA channels	12	12	12
CAN interface	2	2	1
Configurable Custom Logic (CCL) (LUTs)	4	4	4
Serial Communication Interface (SERCOM) instances	6	6	4
Analog-to-Digital Converter (ADC) instances	2	2	2
Analog-to-Digital Converter (ADC) channels	20	14	10
Sigma-Delta Analog-to-Digital Converter (SDADC) channels	3	2	1
Analog Comparators (AC)	4	4	3
Digital-to-Analog Converter (DAC) channels	1	1	1
Real-Time Counter (RTC)	Yes	Yes	Yes
RTC alarms	1	1	1
RTC compare values	1 32-bit value or 2 16-bit values	1 32-bit value or 2 16-bit values	1 32-bit value or 2 16-bit values
External Interrupt lines	16	16	16
Peripheral Touch Controller (PTC) X and Y lines	16x16	12x10	10x6
Maximum CPU frequency	48MHz		
Packages	QFN TQFP	QFN TQFP	QFN TQFP

	SAM C21J	SAM C21G	SAM C21E
Oscillators	32.768kHz crystal oscillator (XOSC32K) 0.4-32MHz crystal oscillator (XOSC) 32.768kHz internal oscillator (OSC32K) 32kHz ultra-low-power internal oscillator (OSCULP32K) 48MHz high-accuracy internal oscillator (OSC48M) 96MHz Fractional Digital Phased Locked Loop (FDPLL96M)		
Event System channels	12	12	12
SW Debug Interface	Yes	Yes	Yes
Watchdog Timer (WDT)	Yes	Yes	Yes

2. Ordering Information



2.1 SAM C21E

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMC21E15A-AUT	32K	4K	TQFP32	Tape & Reel
ATSAMC21E15A-MUT	32K	4K	QFN32	Tape & Reel
ATSAMC21E16A-AUT	64K	8K	TQFP32	Tape & Reel
ATSAMC21E16A-MUT	64K	8K	QFN32	Tape & Reel
ATSAMC21E17A-AUT	128K	16K	TQFP32	Tape & Reel
ATSAMC21E17A-MUT	128K	16K	QFN32	Tape & Reel
ATSAMC21E18A-AUT	256K	32K	TQFP32	Tape & Reel
ATSAMC21E18A-MUT	256K	32K	QFN32	Tape & Reel

2.2 SAM C21G

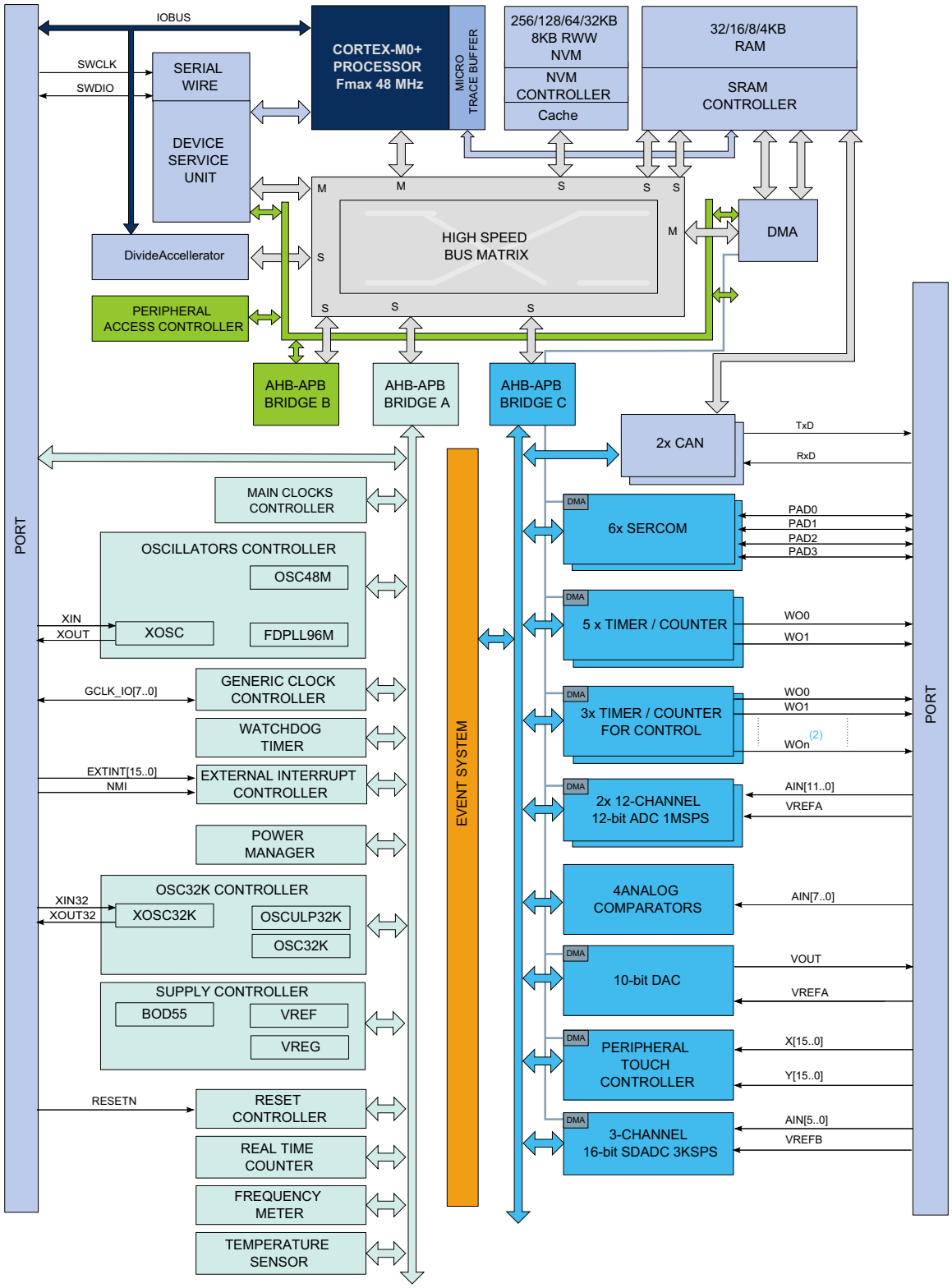
Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMC21G15A-AUT	32K	4K	TQFP48	Tape & Reel
ATSAMC21G15A-MUT	32K	4K	QFN48	Tape & Reel
ATSAMC21G16A-AUT	64K	8K	TQFP48	Tape & Reel
ATSAMC21G16A-MUT	64K	8K	QFN48	Tape & Reel

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMC21G17A-AUT	128K	16K	TQFP48	Tape & Reel
ATSAMC21G17A-MUT	128K	16K	QFN48	Tape & Reel
ATSAMC21G18A-AUT	256K	32K	TQFP48	Tape & Reel
ATSAMC21G18A-MUT	256K	32K	QFN48	Tape & Reel

2.3 SAM C21J

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMC21J15A-AUT	32K	4K	TQFP64	Tape & Reel
ATSAMC21J15A-MUT	32K	4K	QFN64	Tape & Reel
ATSAMC21J16A-AUT	64K	8K	TQFP64	Tape & Reel
ATSAMC21J16A-MUT	64K	8K	QFN64	Tape & Reel
ATSAMC21J17A-AUT	128K	16K	TQFP64	Tape & Reel
ATSAMC21J17A-MUT	128K	16K	QFN64	Tape & Reel
ATSAMC21J18A-AUT	256K	32K	TQFP64	Tape & Reel
ATSAMD20J18A-MUT	256K	32K	QFN64	Tape & Reel

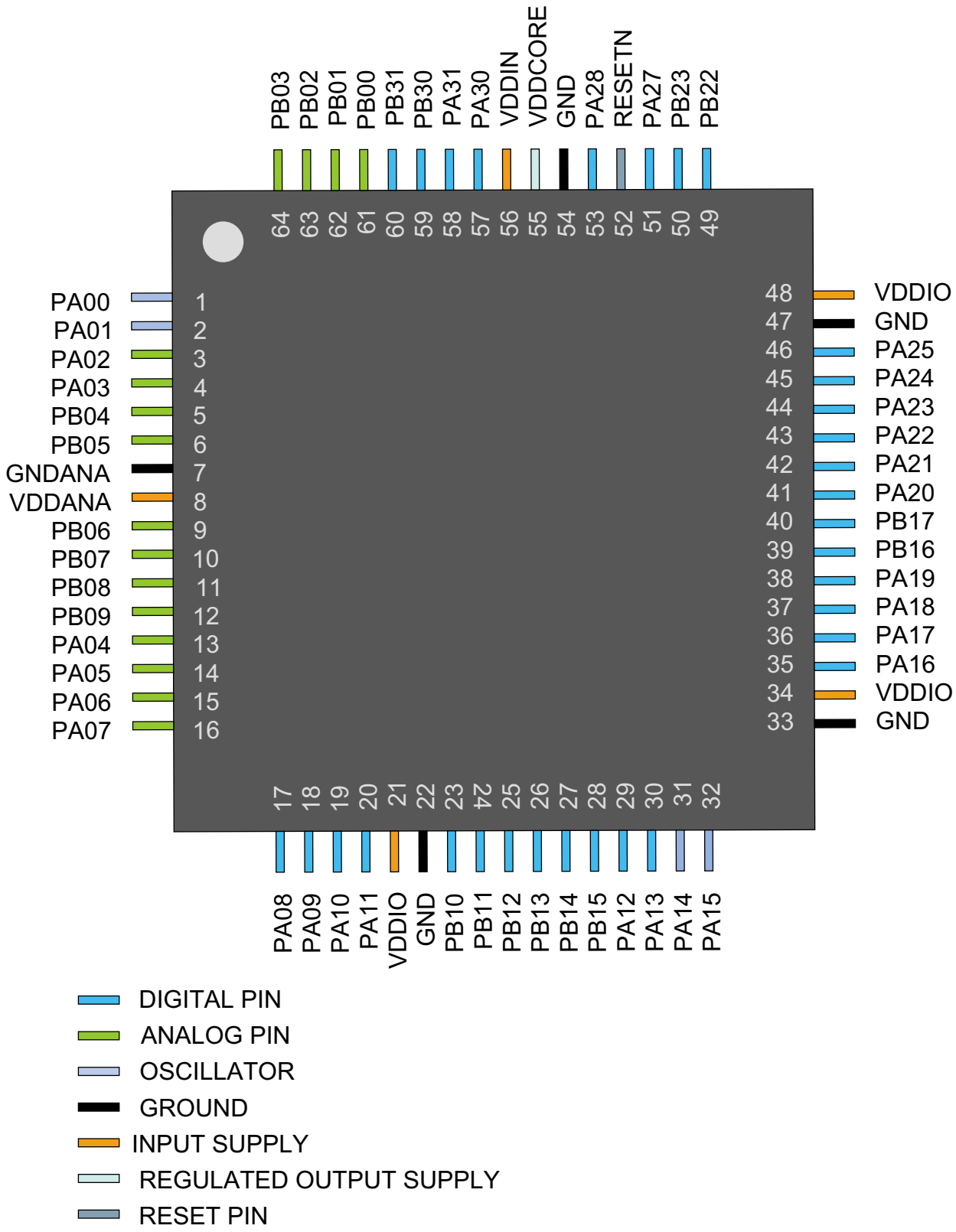
3. Block Diagram



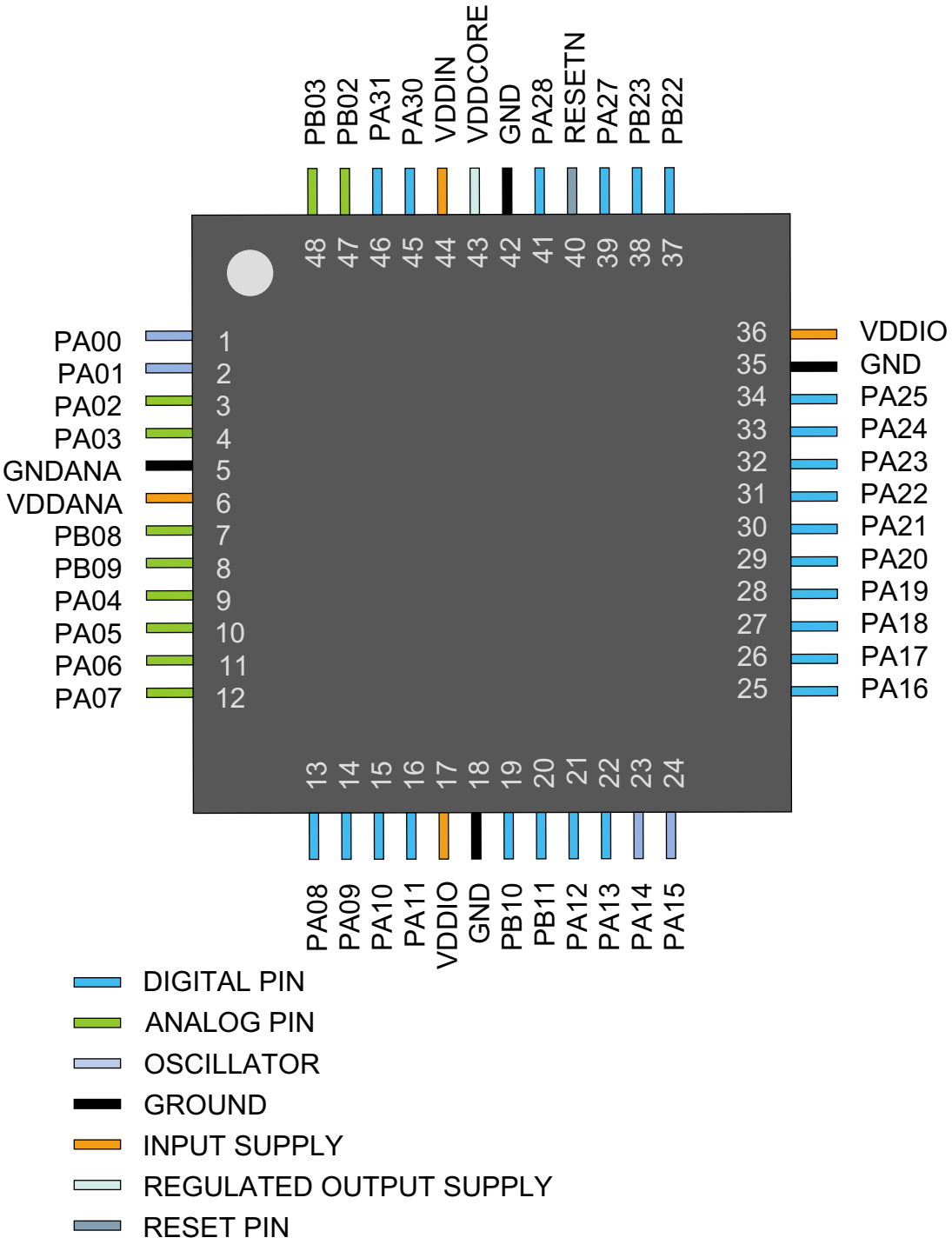
Notes:
1. Some products have different number of SERCOM instances, Timer/Counter instances, PTC signals and ADC signals. Refer to "Ordering Information" on page 4 for details.
2. The three TCC instances have different configurations, including the number of Waveform Output (WO) lines. Refer to !!!CRT_TCC_Config!!! for details.

4. Pinout

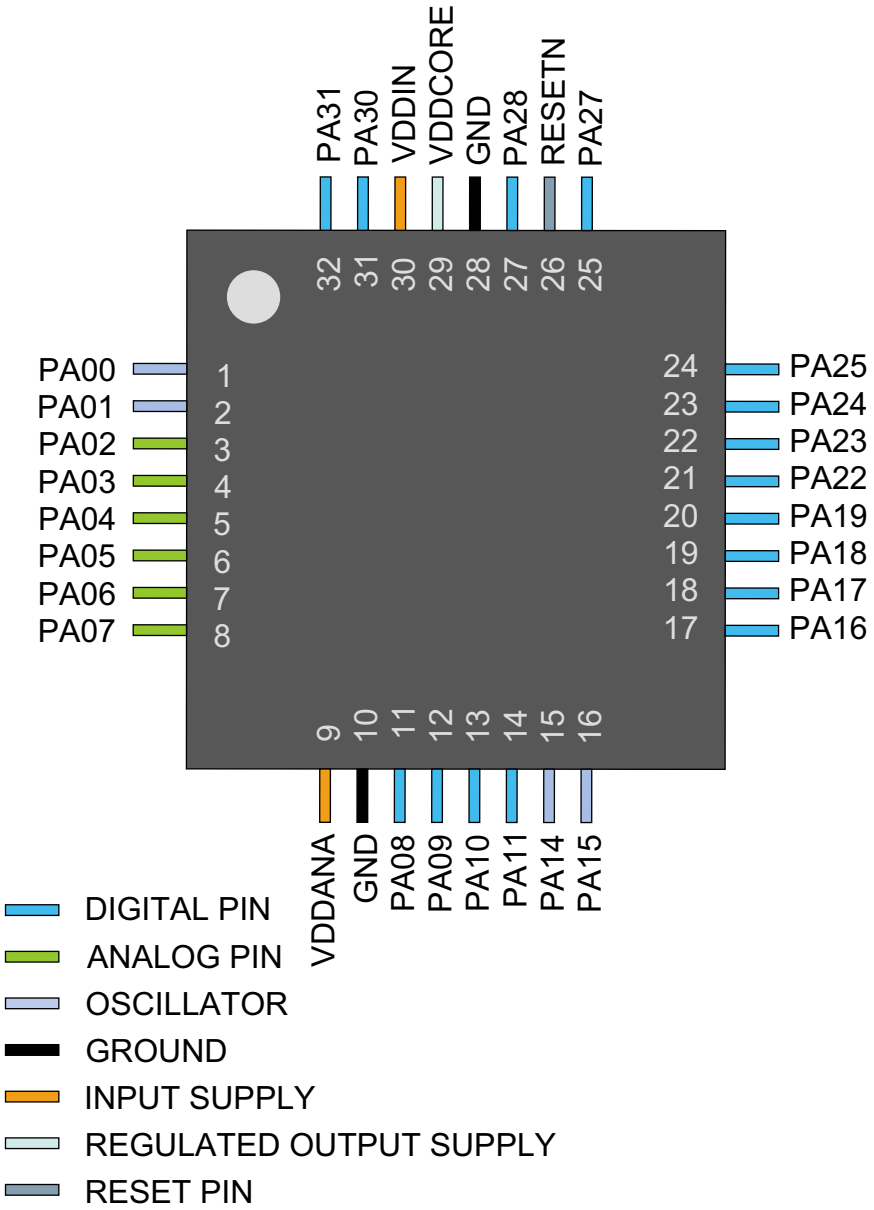
4.1 SAM C21J



4.2 SAM C21G


PB03
PB02
PA31
PA30
VDDIN
VDDCORE
GND
PA28
RESETN
PA27
PB23
PB22
48
47
46
45
44
43
42
41
40
39
38
37
PA00 1
PA01 2
PA02 3
PA03 4
GNDANA 5
VDDANA 6
PB08 7
PB09 8
PA04 9
PA05 10
PA06 11
PA07 12
36 VDDIO
35 GND
34 PA25
33 PA24
32 PA23
31 PA22
30 PA21
29 PA20
28 PA19
27 PA18
26 PA17
25 PA16
13
14
15
16
17
18
19
20
21
22
23
24
PA08
PA09
PA10
PA11
VDDIO
GND
PB10
PB11
PA12
PA13
PA14
PA15
DIGITAL PIN
ANALOG PIN
OSCILLATOR
GROUND
INPUT SUPPLY
REGULATED OUTPUT SUPPLY
RESET PIN

4.3 SAM C21E


PA31
PA30
VDDIN
VDDCORE
GND
PA28
RESETN
PA27
32
31
30
29
28
27
26
25
PA00
PA01
PA02
PA03
PA04
PA05
PA06
PA07
1
2
3
4
5
6
7
8
24
23
22
21
20
19
18
17
PA25
PA24
PA23
PA22
PA19
PA18
PA17
PA16
9
10
11
12
13
14
15
16
VDDANA
GND
PA08
PA09
PA10
PA11
PA14
PA15
DIGITAL PIN
ANALOG PIN
OSCILLATOR
GROUND
INPUT SUPPLY
REGULATED OUTPUT SUPPLY
RESET PIN

5. Processor And Architecture

5.1 Cortex M0+ Processor

The Atmel|SMART SAM C21 implements the ARM® Cortex™-M0+ processor, based on the ARMv6 Architecture and Thumb®-2 ISA. The Cortex M0+ is 100% instruction set compatible with its predecessor, the Cortex-M0 core, and upward compatible to Cortex-M3 and M4 cores. For more information refer to www.arm.com.

5.1.1 Cortex M0+ Configuration

Features	Configurable option	Atmel|SMART SAM C21 configuration
Interrupts	External interrupts 0-32	32
Data endianness	Little-endian or big-endian	Little-endian
SysTick timer	Present or absent	Present
Number of watchpoint comparators	0, 1, 2	2
Number of breakpoint comparators	0, 1, 2, 3, 4	4
Halting debug support	Present or absent	Present
Multiplier	Fast or small	Fast (single cycle)
Single-cycle I/O port	Present or absent	Present
Wake-up interrupt controller	Supported or not supported	Not supported
Vector Table Offset Register	Present or absent	Present
Unprivileged/Privileged support	Present or absent	Present
Memory Protection Unit	Not present or 8-region	8-region
Reset all registers	Present or absent	Absent
Instruction fetch width	16-bit only or mostly 32-bit	32-bit

The ARM Cortex-M0+ core has two bus interfaces:

- Single 32-bit AMBA-3 AHB-Lite system interface that provides connections to peripherals and all system memory, which includes flash and RAM
- Single 32-bit I/O port bus interfacing to the PORT and DIVA with 1-cycle loads and stores

6. Packaging Information

6.1 Thermal Considerations

6.1.1 Thermal Resistance Data

Table 6-1 on page 13 summarizes the thermal resistance data depending on the package.

Table 6-1. Thermal Resistance Data

Package Type	θ_{JA}	θ_{JC}
32-pin TQFP	68 °C/W	25.8 °C/W
48-pin TQFP	78.8 °C/W	12.3 °C/W
64-pin TQFP	66.7 °C/W	11.9 °C/W
32-pin QFN	37.2 °C/W	3.1 °C/W
48-pin QFN	33 °C/W	11.4 °C/W
64-pin QFN	33.5 °C/W	11.2 °C/W

6.1.2 Junction Temperature

The average chip-junction temperature, T_J, in °C can be obtained from the following:

1. $T_D = T_A + (P_D \times \theta_{JA})$
2. $T_D = T_A + (P_D \times (\theta_{HEATSINK} + \theta_{JC}))$

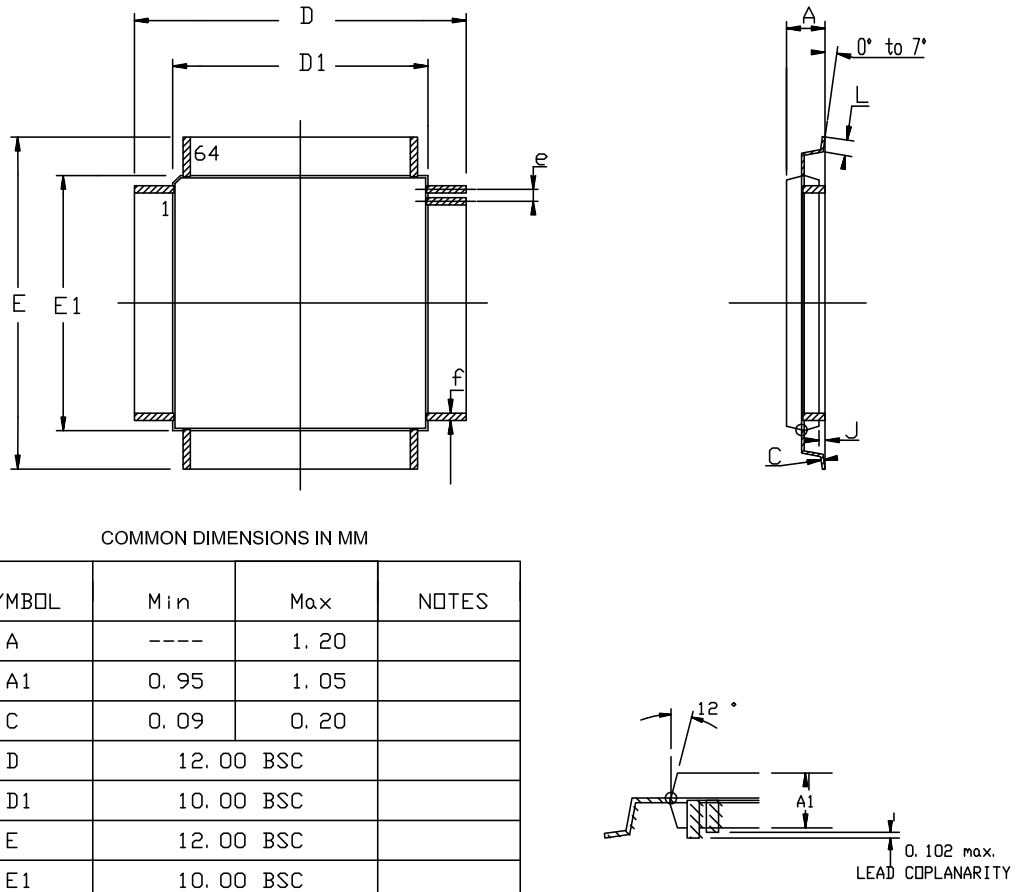
where:

- θ_{JA} = package thermal resistance, Junction-to-ambient (°C/W), provided in Table 6-1 on page 13.
- θ_{JC} = package thermal resistance, Junction-to-case thermal resistance (°C/W), provided in Table 6-1 on page 13.
- $\theta_{HEATSINK}$ = cooling device thermal resistance (°C/W), provided in the device datasheet.
- P_D = device power consumption (W).
- T_A = ambient temperature (°C).

From the first equation, the user can derive the estimated lifetime of the chip and decide if a cooling device is necessary or not. If a cooling device is to be fitted on the chip, the second equation should be used to compute the resulting average chip-junction temperature T_J in °C.

6.2 Package Drawings

6.2.1 64-pin TQFP



COMMON DIMENSIONS IN MM

SYMBOL	Min	Max	NOTES
A	----	1.20	
A1	0.95	1.05	
C	0.09	0.20	
D	12.00 BSC		
D1	10.00 BSC		
E	12.00 BSC		
E1	10.00 BSC		
J	0.05	0.15	
L	0.45	0.75	
e	0.50 BSC		
f	0.17	0.27	

Table 6-2. Device and Package Maximum Weight

300	mg

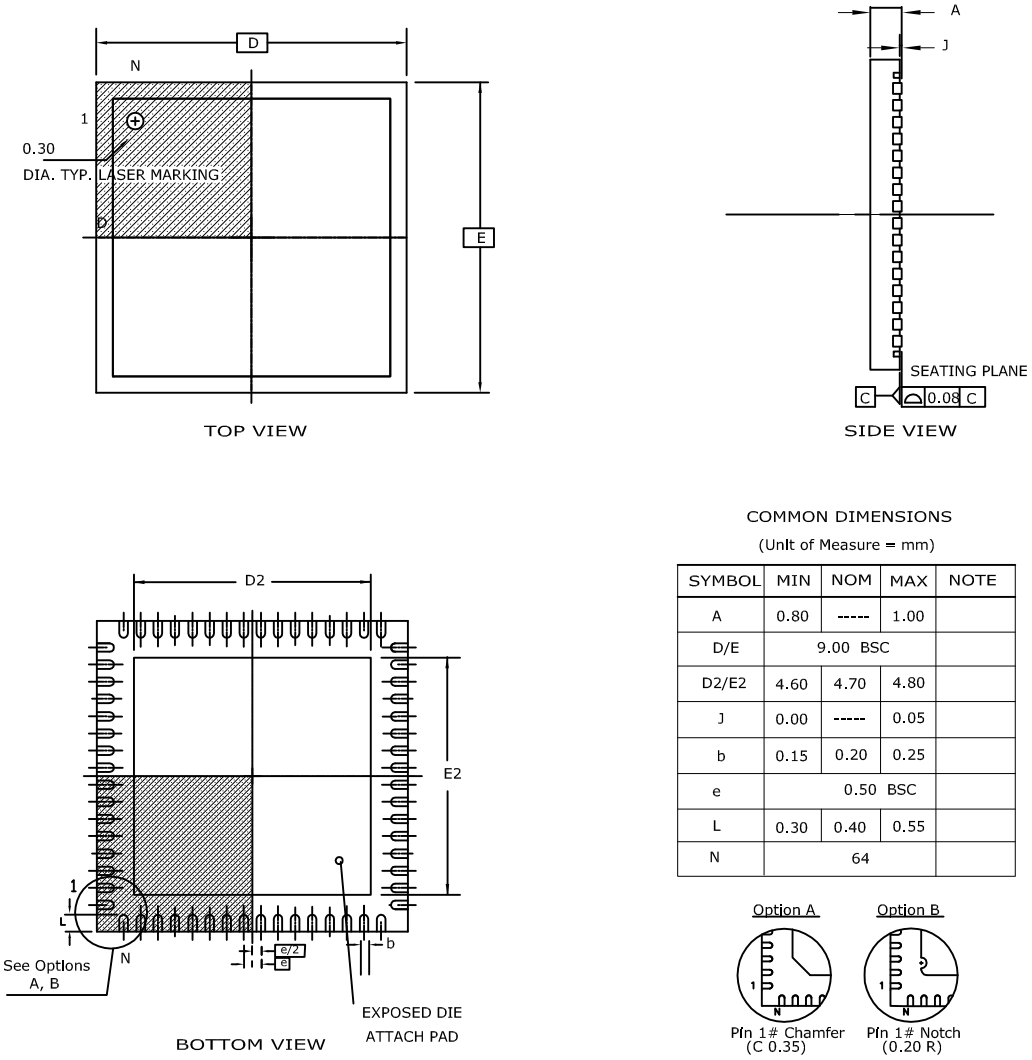
Table 6-3. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 6-4. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

6.2.2 64-pin QFN



COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	-----	1.00	
D/E		9.00 BSC		
D2/E2	4.60	4.70	4.80	
J	0.00	-----	0.05	
b	0.15	0.20	0.25	
e		0.50 BSC		
L	0.30	0.40	0.55	
N		64		

Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MO-220, Variation VMMD-4, for proper dimensions, tolerances, datums, etc.
2. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
If the terminal has the optical radius on the other end of the terminal, the dimension should not be measured in that radius area.

Table 6-5. Device and Package Maximum Weight

200	mg

Table 6-6. Package Characteristics

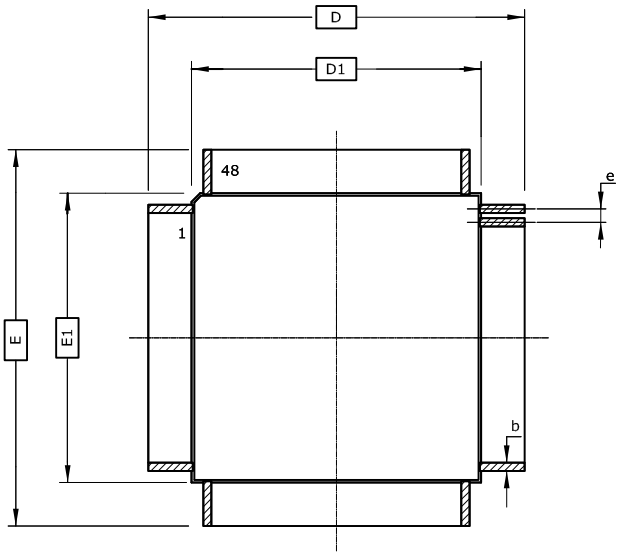
Moisture Sensitivity Level	MSL3

Table 6-7. Package Reference

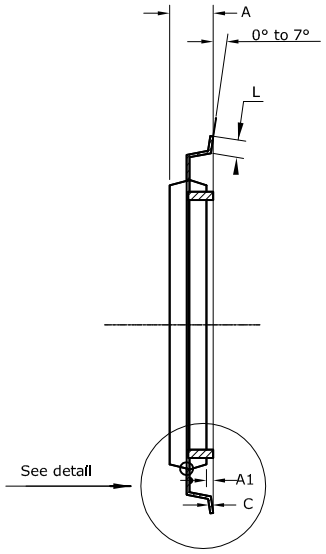
JEDEC Drawing Reference	MO-220
JESD97 Classification	E3

6.2.3 48-pin TQFP

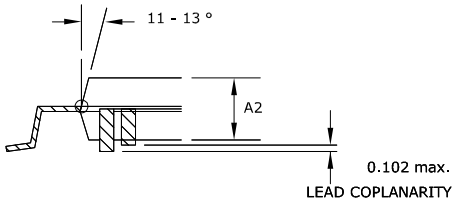
DRAWINGS NOT SCALED



TOP VIEW



SIDE VIEW



DETAIL VIEW

COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-----	-----	1.20	
A1	0.05	-----	0.15	
A2	0.95	-----	1.05	
C	0.09	-----	0.20	
D/E	9.00 BSC			
D1/E1	7.00 BSC			
L	0.45	-----	0.75	
b	0.17	-----	0.27	
e	0.50 BSC			

Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MS-026, Variation ABC.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

Table 6-8. Device and Package Maximum Weight

140	mg

Table 6-9. Package Characteristics

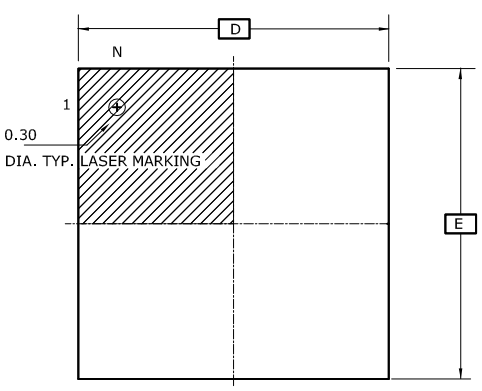
Moisture Sensitivity Level	MSL3

Table 6-10. Package Reference

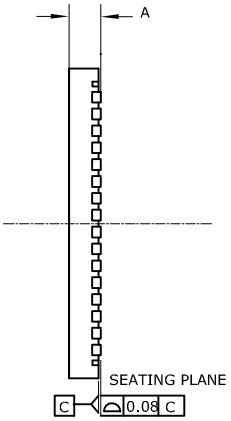
JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

6.2.4 48-pin QFN

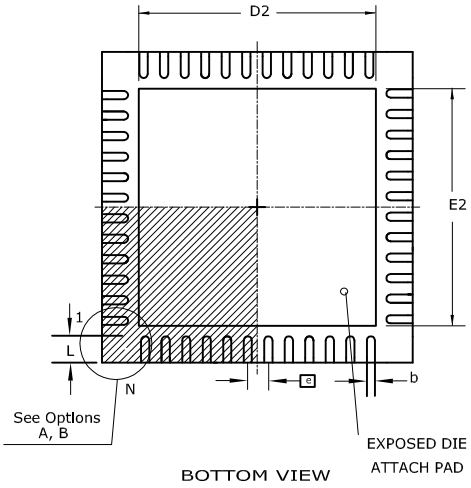
DRAWINGS NOT SCALED



TOP VIEW



SIDE VIEW

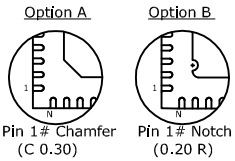


BOTTOM VIEW

COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.85	0.90	
D/E		7.00 BSC		
D2/E2	5.05	5.15	5.25	
b	0.18	0.25	0.30	
e		0.50 BSC		
L	0.30	0.40	0.50	
N		48		



Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MO-220, Variation VKKD-4, for proper dimensions, tolerances, datums, etc.
2. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
If the terminal has the optical radius on the other end of the terminal, the dimension should not be measured in that radius area.

Table 6-11. Device and Package Maximum Weight

140	mg

Table 6-12. Package Characteristics

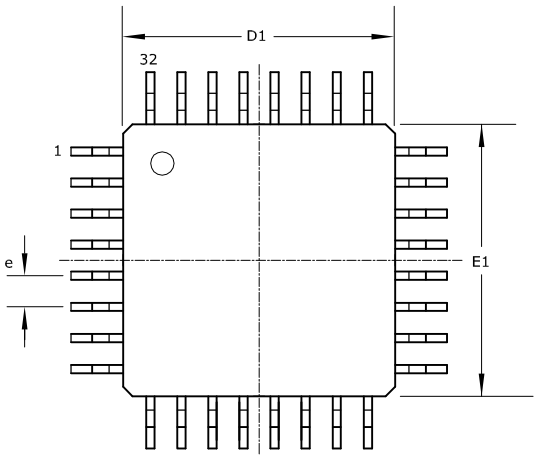
Moisture Sensitivity Level	MSL3

Table 6-13. Package Reference

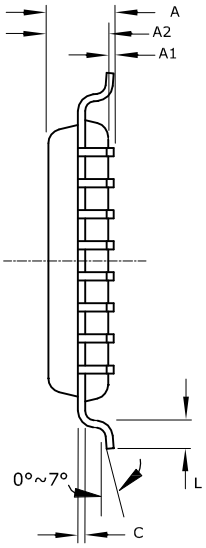
JEDEC Drawing Reference	MO-220
JESD97 Classification	E3

6.2.5 32-pin TQFP

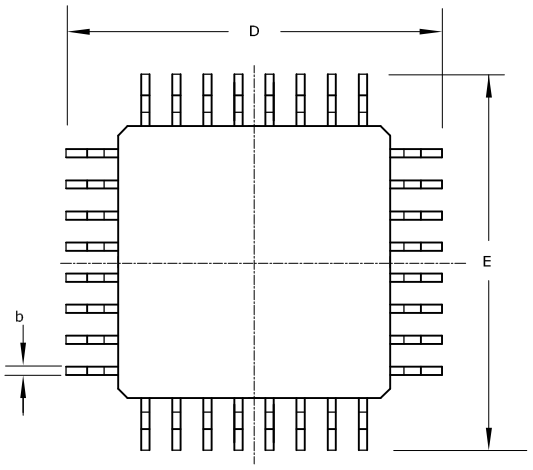
DRAWINGS NOT SCALED



TOP VIEW



SIDE VIEW



BOTTOM VIEW

COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-----	-----	1.20	
A1	0.05	-----	0.15	
A2	0.95	1.00	1.05	
D/E	8.75	9.00	9.25	
D1/E1	6.90	7.00	7.10	2
C	0.09	-----	0.20	
L	0.45	-----	0.75	
b	0.30	-----	0.45	
e	0.80 TYP			
n	32			

Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MS-026, Variation ABA.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

Table 6-14. Device and Package Maximum Weight

100	mg

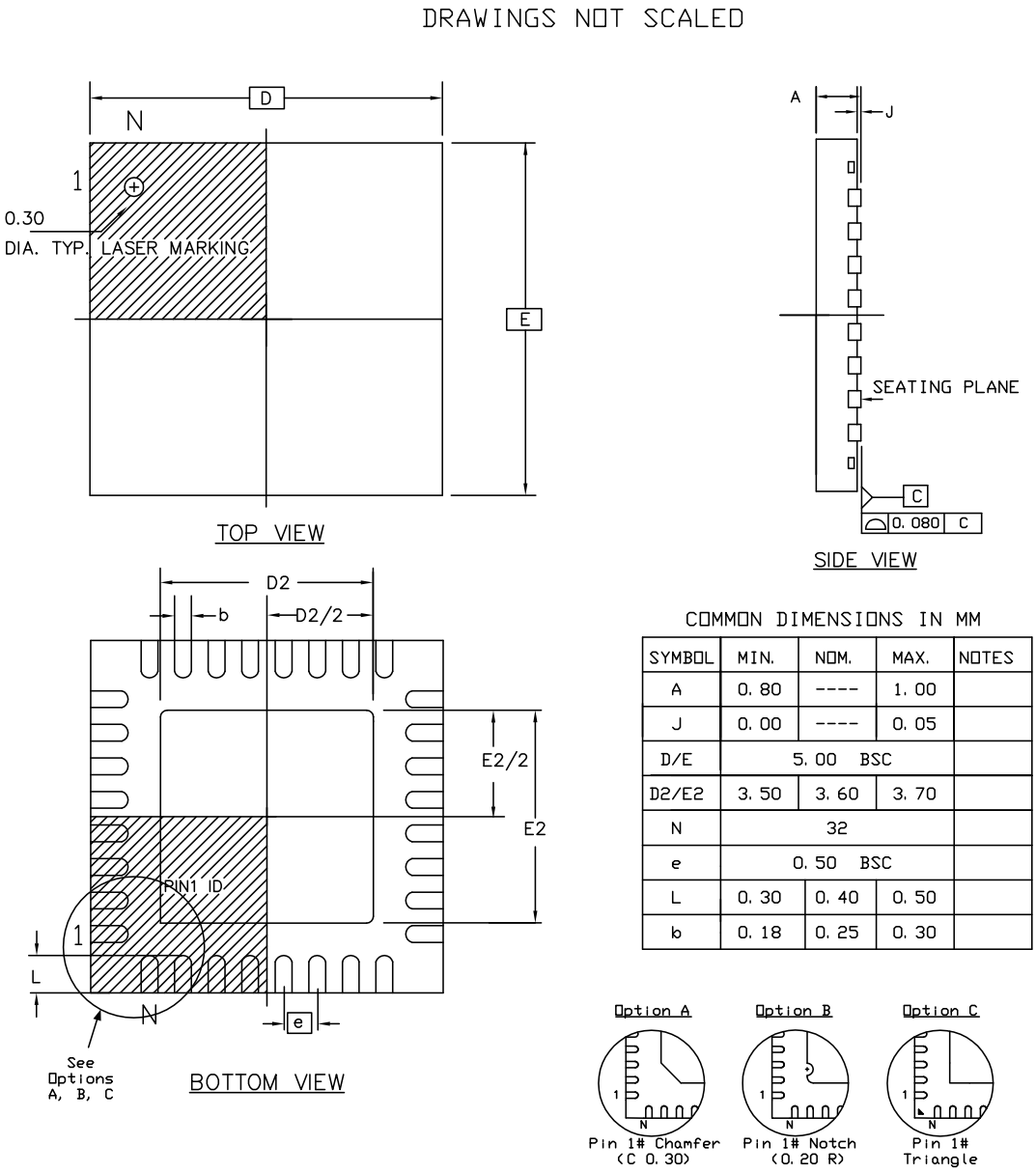
Table 6-15. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 6-16. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

6.2.6 32-pin QFN



SYMBOL	MIN.	NOM.	MAX.	NOTES
A	0.80	----	1.00	
J	0.00	----	0.05	
D/E		5.00 BSC		
D2/E2	3.50	3.60	3.70	
N		32		
e		0.50 BSC		
L	0.30	0.40	0.50	
b	0.18	0.25	0.30	

Table 6-17. Device and Package Maximum Weight

90	mg

Table 6-18. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 6-19. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E3

6.3 Soldering Profile

The following table gives the recommended soldering profile from J-STD-20.

Profile Feature	Green Package
Average Ramp-up Rate (217°C to peak)	3°C/s max
Preheat Temperature 175°C +/-25°C	150-200°C
Time Maintained Above 217°C	60-150s
Time within 5°C of Actual Peak Temperature	30s
Peak Temperature Range	260°C
Ramp-down Rate	6°C/s max
Time 25°C to Peak Temperature	8 minutes max

A maximum of three reflow passes is allowed per component.

Table of Contents

Atmel | Enabling Unlimited Possibilities®

Atmel Corporation 1600 Technology Drive, San Jose, CA 95110 USA **T:** (+1)(408) 441.0311 **F:** (+1)(408) 436.4200 | **www.atmel.com**